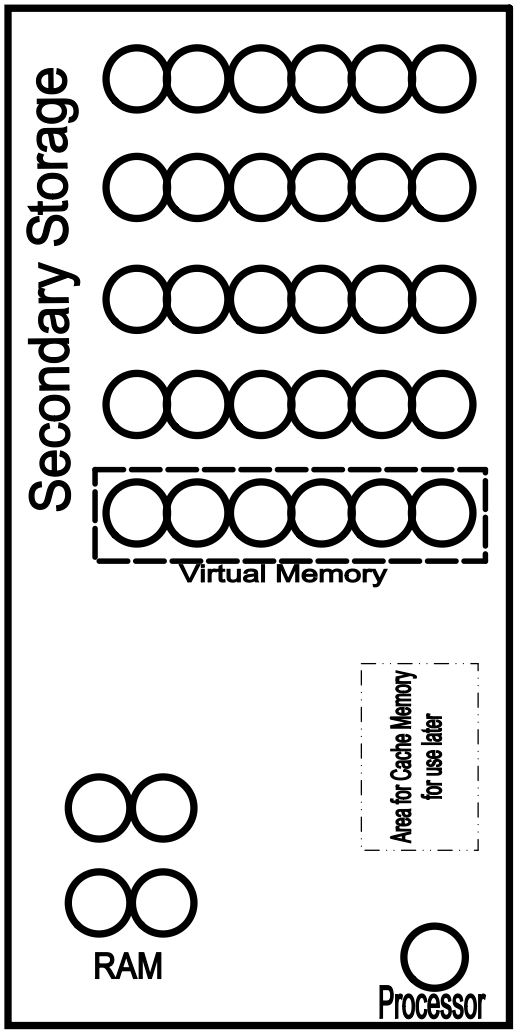
Main Memory – GCSE Activity

Concepts/Terminology Addressed

RAM, Cache Memory, Secondary Storage, Virtual Memory, Access times, Memory Capacity terms

Resources required:

- Numbered pages (one for each student)
- A4 poster/labels for RAM, Secondary Storage, Processor and Cache Memory



Preparation:

Student chairs are arranged in rows at one end of the room, whilst a single chair is placed at other end of the room with a small number (typically 4) of chairs off to the side, somewhere between the two.

It is important to leave an area that will be used to illustrate cache memory later in the exercise.

Students are given a number on a page but then instructed to sit randomly in the rows of chairs that represent secondary storage.

One student is chosen to be the processor and a couple are selected to be the 'buses'; one that must walk slowly in pigeon steps, a second that may walk medium paced and a third who is instructed to move very quickly.

Activity:

Stage 1 : Accessing data from the HDD without the use of RAM

The student who is the processer requests the first instruction, and student who is the slow bus, walking in pigeon steps, must walk over to the secondary storage area walking up and down each row until they find the 1st instruction. At this point they then return to the processor, who then requests the next numbered instruction and the process is repeated. Once this has been repeated a few times to emphasise the slow pace of the data transfer it is then possible to raise the idea of how could it be sped up.

Stage 2 : Loading data from HDD into RAM and accessing it from there

The numbered students/pages are reset (all given back to their original owners) and the students with the first four instructions are moved to the RAM seats. The processor begins repeating the process of requesting instruction, only this time the medium speed bus is used to retrieve the numbers from the students in the RAM chairs. The difference in access time should be emphasised. The slow bus can be used at this point to transfer the next available instruction into the empty RAM seats, albeit at a slower rate.

Stage 3 : Illustrating the use of Cache memory

At this point we might look at our speedy bus and point out that they have had nothing to do yet and use this to introduce the idea of an even smaller area of accessible memory between RAM and the processor, which can be accessed even faster than RAM. Two chairs from the front row can be moved into another area of the room (ideally nearer the processor student than RAM). Reset the numbers with the following arrangements:

- Numbers 1 & 2 in the cache memory seats
- Numbers 3 – 6 in the RAM seats

The processor starts requesting numbers and the fast bus zips along getting them from the cache memory. While this is being done, the medium bus transfers the next instruction from RAM to cache memory (at a slower pace than the fast bus is moving). And the slow bus continues to refill the RAM seats from secondary storage.

Stage 4 : Increasing the amount of RAM to increase speed

Often students will have mentioned that increasing the amount of RAM might help increase the speed of the computer overall. Move some of the chairs from the front row to the RAM area, explaining that you have just installed some additional RAM and the effects that this might have. The processing can then be carried out again, and the students should be able to see that more data is in the faster access area and therefore the impact it has on the overall performance.

Stage 5 : Utilising Virtual Memory to increase speed

The idea of not having enough RAM may have been mentioned by now and this allows the concept of virtual memory to be introduced. After 'resetting' the students again, the next few instructions are rearranged to be on the first row of the secondary storage seats. The process is now repeated, only this time two buses work together. The Slow bus transfers data from the virtual memory seats to the RAM seats and the medium speed bus from RAM to the processor. **(A possible variation on this is that the medium speed bus is told they can visit both the RAM seats and those seats allocated as virtual memory.**

Possible Variations/Extensions:

- Memory addressing
- Fetch Execute Cycle
- Assembly level programming
- Little Man Computer concepts